

**A METHOD FOR ETCHING A SUBSTRATE
AND A DEVICE FORMED USING THE METHOD**

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TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to etching and, more specifically, to a method for etching a substrate using a specific etchant recipe.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits are mass produced by fabricating hundreds of identical circuit patterns on a single semiconductor wafer. One of the many different processes repeated over and over in manufacturing these integrated circuits is that of using a mask and etchant for forming a particular feature. In such a mask and etching process, a photo mask containing the pattern of the structure to be fabricated is created, then, after formation of a material layer within which the feature is to be formed, the material layer is coated with a light-sensitive material called photoresist or resist. The resist-coated material layer is then exposed to ultraviolet light through the mask, thereby transferring the pattern from the mask to the resist. The wafer is then etched to remove the material layer unprotected by the resist, and then

the remaining resist is stripped. This masking process permits specific areas of the material layer to be formed to meet the desired device design requirements.

[0003] In the etching process described above, it is important that the etching selectively remove the unwanted material and that the material underlying the material layer is not excessively damaged. A common way to accomplish this is to deposit or otherwise form an etch stop layer on the wafer prior to formation of the material layer. Such etch stop layers are commonly made of a material that is resistant to the particular etching process used.

[0004] In the integrated circuit fabrication art, the property of being resistant to an etching process is called the "selectivity" of a material. The selectivity of a particular material in a particular etching process is usually defined as the etching rate of the material to be removed divided by the etching rate of the particular material. Thus, a material that is highly resistant to an etch is said to have a high selectivity.

[0005] One of the most effective, and thus common etch stop layers currently used in the fabrication of integrated circuits is silicon nitride (SiN). Unfortunately, using SiN as the etch stop layers introduces unwanted hydrogen into the features of the integrated circuits. Hydrogen is unwanted for a number of reasons. First, the unwanted hydrogen has a negative impact on the

transistors, often affecting their gate oxide integrity (GOI) value, antenna gate leakage value, threshold voltage drift value, negative bias temperature instability (NBTI) value, etc. Second, when used in conjunction with ferroelectric memory cells, the unwanted hydrogen introduced by the SiN is often catastrophic. For this reason, a barrier layer is typically introduced between the ferroelectric memory cell and the SiN etch stop. Regrettably, the barrier layer provides an additional step to the already complicated manufacturing process.

[0006] Accordingly, what is needed in the art is an etch stop that does not experience, or in another aspect introduce, the problems that arise with the use of the prior art etch stops.

SUMMARY OF THE INVENTION

[0007] To address the above-discussed deficiencies of the prior art, the present invention provides a method for etching a substrate, a method for forming an integrated circuit and an integrated circuit formed using the method. The method for etching a substrate includes, among other steps, providing a substrate having an aluminum oxide etch stop layer located thereunder, and then etching an opening in the substrate using an etchant comprising a carbon oxide, a fluorocarbon, an etch rate modulator, and an inert carrier gas, wherein a flow rate of the carbon oxide is greater than about 80 sccm and the etchant is selective to the aluminum oxide etch stop layer.

[0008] As indicated above, the present invention further provides a method for forming an integrated circuit. The method for forming the integrated circuit may include providing semiconductor devices over a semiconductor substrate and providing a dielectric layer over the semiconductor devices, the dielectric layer having an aluminum oxide etch stop layer located thereunder. The method may further include etching openings in the dielectric layer using an etchant comprising a carbon oxide, a fluorocarbon, an etch rate modulator, and an inert carrier gas, wherein a flow rate of the carbon oxide is greater than about 80 sccm and the etchant is selective to the aluminum oxide etch stop layer, and

contacting the semiconductor devices through the openings.

[0009] The foregoing has outlined preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The invention is best understood from the following detailed description when read with the accompanying FIGURES. It is emphasized that in accordance with the standard practice in the semiconductor industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0011] FIGURE 1A illustrates a cross-sectional view of a semiconductor device manufactured according to the principles of the present invention;

[0012] FIGURE 1B illustrates an SEM image of a device similar to the semiconductor device illustrated in FIGURE 1A;

[0013] FIGURE 2 illustrates a cross-sectional view of a partially completed semiconductor device;

[0014] FIGURE 3 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 2 after conventionally forming a dielectric layer over the microelectronic device and aluminum oxide etch stop layer;

[0015] FIGURE 4 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 3 after etching openings within the dielectric layer;

[0016] FIGURE 5 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 4 after conventional removal of the remaining aluminum oxide etch stop layer within the openings;

[0017] FIGURE 6 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 5 after conventionally forming conductive plugs within the openings; and

[0018] FIGURE 7 illustrates a cross-sectional view of an integrated circuit (IC) incorporating semiconductor devices constructed according to the principles of the present invention.

DETAILED DESCRIPTION

[0019] Referring initially to FIGURE 1A illustrated is a cross-sectional view of a semiconductor device 100 manufactured according to the principles of the present invention. The semiconductor device 100 of the embodiment of FIGURE 1A includes a ferroelectric capacitor 120 formed over a substrate 110. Located over the ferroelectric capacitor 120 is an aluminum oxide etch stop layer 130. In the exemplary embodiment of FIGURE 1A, the aluminum oxide etch stop layer 130 is also located over and in contact with the substrate 110. While the aluminum oxide etch stop layer 130 is labeled as an etch stop layer, uniquely, it also acts as a diffusion barrier layer protecting the ferroelectric capacitor 120 from unwanted contaminants. Thus, the aluminum oxide etch stop layer 130 ultimately functions as a dual purpose etch stop/barrier layer.

[0020] Located over the aluminum oxide etch stop layer 130 and ferroelectric capacitor 120 is a dielectric layer 140, such as an interlevel dielectric layer. Located within the dielectric layer 140 are openings 150, 155, such as contact holes, vias, trenches, etc. The openings 150, 155, in accordance with the principles of the present invention, were formed using an etchant comprising a carbon oxide, a fluorocarbon, an etch rate modulator, and an inert carrier gas, wherein a flow rate of the carbon oxide is greater

than about 80 sccm, and exemplary greater than about 125 sccm. The aforementioned etchant recipe allows the etchant to be selective to the aluminum oxide etch stop layer 130, while easily etching the openings 150, 155, in the dielectric layer 140. This is particularly useful as the openings 150, 155, are generally simultaneously formed, and the opening 155 must etch deeper than the opening 150 without the opening 150 overetching into the ferroelectric capacitor 120. The combination of the aluminum oxide etch stop layer 130 and the specific etchant recipe allows this stair-stepped multiple trench structure, as shown in FIGURE 1A, to be easily formed.

[0021] Turning briefly to FIGURE 1B, illustrated is an SEM image 190 of a device similar to the semiconductor device 100 illustrated in FIGURE 1A. As illustrated in the SEM image 190, the etching of the opening 150 terminates at the aluminum oxide etch stop layer 130 without substantially overetching into the ferroelectric capacitor 120. Prior to the present invention, such a selectivity was not generally attainable without the use of a silicon nitride (SiN) etch stop layer, which as previously indicated, introduces unwanted hydrogen into the manufacturing process.

[0022] Returning to the embodiment of FIGURE 1A, located within the openings 150, 155, are conductive plugs 160. Optionally located over the dielectric layer 140 is a diffusion barrier layer 170. The diffusion barrier layer 170, which may comprise aluminum

oxide or another similar barrier material, attempts to prevent the migration of unwanted contaminants within the semiconductor device 100. Located over the diffusion barrier layer 170 is another dielectric layer 180 and another optional diffusion barrier layer 190. The additional dielectric layer 180 and additional optional diffusion barrier layer 190 may comprise similar materials to the dielectric layer 140 and optional diffusion barrier layer 170, respectively.

[0023] While not shown, those skilled in the art understand that the diffusion barrier layers 170, 190, alone or in combination could be used in a conventional CMOS process, for example without the ferroelectric capacitor 120 located therein. As the diffusion barrier layers 170, 190, may comprise aluminum oxide, and may function as etch stop layers, they do not introduce the unwanted hydrogen into the manufacturing process as conventional silicon nitride etch stop layers might. Accordingly, in an alternative embodiment of the present invention, all the silicon nitride etch stop layers conventionally used within the aforementioned conventional CMOS process might be replaced with aluminum oxide diffusion barrier layers. Those aluminum oxide diffusion barrier layers, therefore, could be located in the back-end of the manufacturing process where hydrogen is commonly introduced. Therefore, the aluminum oxide diffusion barrier layers might be used for diffusion prevention purposes, as well as eliminating the

hydrogen typically introduced by the conventional silicon nitride etch stop layer manufacturing processes.

[0024] Turning now to FIGURES 2-5, illustrated are cross-sectional views of detailed manufacturing steps instructing how one might, in an advantageous embodiment, manufacture a semiconductor device similar to the semiconductor device 100 depicted in FIGURE 1A. FIGURE 2 illustrates a cross-sectional view of a partially completed semiconductor device 200. The partially completed semiconductor device 200 includes a substrate 210. The substrate 210 may, in an exemplary embodiment, be any layer located in the partially completed semiconductor device 200, including a wafer itself or a layer located above the wafer (e.g., epitaxial layer). In the embodiment illustrated in FIGURE 2, the substrate 210 is a dielectric layer, such as an interlevel dielectric layer.

[0025] Located over the substrate 210 in the embodiment depicted in FIGURE 2 is a microelectronic device 220. While the microelectronic device 200 shown in FIGURE 2 happens to be a ferroelectric capacitor, those skilled in the art understand that a number of different types of devices could be substituted for the ferroelectric capacitor and stay within the scope of the present invention. Nonetheless, the microelectronic device 200 will be illustrated as a ferroelectric capacitor for the remaining portion of this document.

[0026] Furthermore, formed over the microelectronic device 220

and portions of the substrate 210 is an aluminum oxide etch stop layer 230. The aluminum oxide etch stop layer 230 may have a number of different stoichiometric compositions as represented by the equation AlO_x . Nonetheless, a stoichiometric composition where x ranges from about 1 to about 2 is most common.

[0027] In the embodiment of FIGURES 2-5, the aluminum oxide etch stop layer 230 has a thickness of greater than about 40 nm, and particularly a thickness ranging from about 40 nm to about 100nm. This thickness, however, is often dependent on the amount of protection the device thereunder requires in view of the etching process. While the aluminum oxide etch stop layer 230 may be formed using a number of different well-known processes, it has been observed that an atomic layer deposition (ALD) process provides the robustness required for many applications of the present invention.

[0028] Turning now to FIGURE 3, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 2 after conventionally forming a dielectric layer 310 over the microelectronic device 220 and aluminum oxide etch stop layer 230. The dielectric layer 310, which most likely represents an interlevel dielectric layer, may comprise a variety of different materials while staying within the scope of the present invention. For instance, any known or hereafter discovered dielectric material, including silicon dioxide, could be used for

the dielectric layer 310. As those skilled in the art are well aware, the particular manufacturing process and parameters of the dielectric layer 310 will vary according to its intended use.

[0029] Turning now to FIGURE 4, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 3 after etching openings 410, 420, within the dielectric layer 310. As is indicated in the embodiment of FIGURE 4, the openings 410, 420, are formed having different depths, and each terminate on the aluminum oxide etch stop layer 230. In practice, the etchant may penetrate the aluminum oxide etch stop layer 230 a small amount. Thus, when it is stated that the etch stops "on" the aluminum oxide etch stop layer 230, the word "on" includes both the case where the etch goes to the aluminum oxide etch stop layer 230 and stops and the case where it also to some degree etches the aluminum oxide etch stop layer 230 and stops in the aluminum oxide etch stop layer 230. Nevertheless, without the aluminum oxide etch stop layer 230, in combination with the specialized etchant recipe used to etch the openings 410, 420, the opening 410 would overetch into the microelectronic device 220 as the opening 420 continues to etch to the surface of the substrate 210. If this overetching were to occur within the opening 410, it could severely harm, or possibly destroy, the microelectronic device 220 located thereunder.

[0030] The etchant recipe used to etch the openings 410, 420, is

substantially different from conventional etchant recipes. For example, the etchant recipe used to etch the openings 410, 420, comprises a carbon oxide, a fluorocarbon, an etch rate modulator, and an inert carrier gas, wherein a flow rate of the carbon oxide is greater than about 80 sccm, and exemplary greater than about 125 sccm. This specific flow rate, in combination with other tailored factors, allows the etchant to stop on the aluminum oxide etch stop layer 230 without overetching into the microelectronic device 220. In one instance, it has been observed that setting the flow rate for the carbon oxide, such as carbon monoxide, to range from about 150 sccm to about 220 sccm provides superior results.

[0031] Depending on the specific type of dielectric layer 310 being etched, the composition for each of the carbon oxide, fluorocarbon, etch rate modulator, and inert carrier gas may change. For example, it is believed that the carbon oxide may be either CO or CO₂. Additionally, while many fluorocarbons may be used, it is believed that C₄F₈ or C₅F₈ provide particularly beneficial results. Other fluorocarbons that might be used, however, include without limitation, C₄F₆, C₂F₆, CF₄, NF₃, XeF₂, F₂, CHF₃, CH₂F₂, CH₃F, SF₆, or any combination thereof.

[0032] The etch rate modulator, among other compositions, may comprise O₂ or N₂. For example, if the dielectric layer 310 comprises OSG, then O₂ cannot be used as the etch rate modulator. Unfortunately, the O₂ tends to leach the carbon from the OSG

dielectric layer. Thus, in this instance N_2 might be used. In those instances where O_2 is used, however, a ratio of the fluorocarbon to the etch rate modulator, in a preferred embodiment, should be at least 2:1. Preferably the ratio would range from about 2:1 to about 3:1, and a flow rate of the fluorocarbon might range from about 12 sccm to about 18 sccm and the flow rate of the etch rate modulator might range from about 4 sccm to about 8 sccm.

[0033] While the specific composition of the etchant may be tailored to stop on the aluminum oxide etch stop layer 230, the time for etching, pressure used during etching and power used for etching may also be tailored. For instance, a pressure ranging from about 50mT to about 150mT might be used, as well as a power ranging from about 1000W to about 1500W might also be used.

[0034] That said, a number of specific etch processes and chemistries have been performed that show high selectivity, in that the etchant stops on the aluminum oxide etch stop layer 230. While many other processes and chemistries exist within the scope of the present invention, a first etchant recipe consisting of 200 CO, 16 C_5F_8 , 6 O_2 and 500 Ar conducted for 90 seconds at 60mT and 1300W performed quite well. Additionally, an etchant recipe consisting of 175 CO, 8 C_5F_8 , 150 N_2 and 800 Ar conducted for 100s at 100mT and 1300W also performed quite well.

[0035] Turning now to FIGURE 5 illustrated is a cross-sectional view of the partially completed semiconductor device 200

illustrated in FIGURE 4 after conventional removal of the remaining aluminum oxide etch stop layer 230 within the openings 410, 420. Those skilled in the art understand the conventional process that might be used to remove the remaining portions of the aluminum oxide etch stop layer 230 within the openings 410, 420, including changing the etchant recipe to a conventional oxide etch recipe.

[0036] Turning now to FIGURE 6 illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 5 after conventionally forming conductive plugs 610 within the openings 410, 420. After the conventional formation of the conductive plugs 610 an optional diffusion barrier layer 620 may be formed over the dielectric layer 310. The diffusion barrier layer 620, which may also comprise aluminum oxide, attempts to reduce the movement of unwanted contaminants within the partially completed semiconductor device 200 illustrated in FIGURE 6. After forming the optional diffusion barrier layer 620 the manufacturing process would continue resulting in a completed semiconductor device, similar to the semiconductor device 100 illustrated in FIGURE 1.

[0037] Referring finally to FIGURE 7, illustrated is a cross-sectional view of an integrated circuit (IC) 700 incorporating semiconductor devices 710 constructed according to the principles of the present invention. The IC 700 may include devices, such as transistors used to form CMOS devices, BiCMOS devices, Bipolar

devices, capacitors or other types of devices. The IC 700 may further include passive devices, such as inductors or resistors, or it may also include optical devices or optoelectronic devices. Those skilled in the art are familiar with these various types of devices and their manufacture. In the particular embodiment illustrated in FIGURE 7, the IC 700 includes the semiconductor devices 710 having dielectric layers 720 formed thereover. Additionally, interconnect structures 730, each including openings 740 and conductive plugs 750, are located within the dielectric layers 720 to interconnect various devices, thus, forming the operational IC 700.

[0038] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.